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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,966	03/31/2004	Scott R. Sahaida	884.C31US1	7702

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EXAMINER	
BRYANT, DELORIS S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,966	SAHAIDA ET AL.	
	Examiner	Art Unit	
	Deloris Bryant	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *12-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 22-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response to non-final rejection canceling claims 12-21 on June 1, 2006 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 7 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Lo et al (US 2003/0160312). Lo discloses a semiconducting device comprising (see Fig. 3): a substrate (102); a first die (104) attached to the substrate (102), the first die including active circuitry on an upper surface; a spacer (124; pg. 3, para 0035) covering the active circuitry on the upper surface (114) of the first die (104), the spacer (124) extending from a first side of the first die to an opposing second side of the first die and extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die (see Fig. 4); and a second die (106) stacked onto the spacer (124) and the first die (105).

Regarding claim 3, Lo discloses wherein the spacer (124) is attached to the upper surface (114) of the first die (104) using an adhesive (126) (pg. 42, para. 0031-0033).

Regarding claims 4 and 5, Lo discloses wherein the spacer (124) includes at least one section that extends to the third side of the first die (104) such that the active circuitry is only partially exposed near the third side of the first die (104) (claim 3) and wherein the spacer (124) includes at least one section that extends to the fourth side of the first die (104) such that the active circuitry is only partially exposed near the fourth side of the first die (claim 4) (see Fig. 4).

Regarding claim 7, Lo discloses wherein the spacer is formed of silicon (pg. 3, para. 0035).

Regarding claim 10, Lo discloses wherein the second die is attached to the spacer using an adhesive (pg. 3, para. 0035).

Regarding claim 11, Lo discloses wires (122) bonded to pads (118) that are part of the exposed active circuitry near the third and fourth sides of the first die (see Fig. 3 and Fig. 4).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 3-5 and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al (US 2005/0194674). Thomas discloses a semiconducting device comprising (see Fig. 1): a substrate (110); a first die (112) attached to the substrate (110), the first die including active circuitry on an upper surface; a spacer (122) covering the active circuitry on the upper surface (116) of the first die (112), the spacer (122) extending from a first side of the first die to an opposing second side of the first die and and a second die (114) stacked onto the spacer (122) and the first die (112). Thomas fails to specifically disclose extending near a third side of the first die and an opposing fourth side of the first die such that the active circuitry is exposed near the third and fourth sides of the first die. It is well known in the art that a quad package would have all four sides of the active circuitry exposed. Although Thomas discloses only two sides of the active circuitry being exposed, it would have been obvious to one skilled in the art at the time of the invention for Thomas to have all four sides exposed. The mere duplication of parts has no patentable significance unless a new and unexpected result is produced. See In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960)

Regarding claim 3, Thomas discloses wherein the spacer (122) is attached to the upper surface (116) of the first die (112) using an adhesive (121) (pg. 4, para. 0047).

Regarding claims 4 and 5, Thomas discloses wherein the spacer (122) includes at least one section that extends to the third side of the first die (112) such that the active circuitry is only partially exposed near the third side of the first die (112) (claim 3) and wherein the spacer (122) includes at least one section that extends to the fourth side of the first die (112) such that the active circuitry is only partially exposed near the fourth side of the first die (claim 4) (see Fig. 1).

Regarding claim 7, Thomas discloses wherein the spacer is formed of silicon (pg. 4, para. 0047).

Regarding claims 8 and 9, Thomas discloses at least one additional die stacked onto the first die, the spacer and the second die (claim 8) and at least one additional die mounted on the substrate, the first die being stacked onto the at least one additional die (claim 9) (pg. 2, para. 0019).

Regarding claim 10, Thomas discloses wherein the second die is attached to the spacer using an adhesive (pg. 4, para. 0050).

Regarding claim 11, Thomas discloses wires (128) bonded to pads (129) that are part of the exposed active circuitry near the third and fourth sides of the first die (see Fig. 1).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al (US 2005,0194674) in view of Katagiri et al (2002/0185744). Thomas discloses all claim limitations in claim 1 above but fails to disclose wherein the first die includes a flash memory array. Katagiri, however, does teach where the first die includes a flash

memory (para. 0069). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the die of Katagiri with the teachings of Thomas because of advantages such as smaller size, lighter weight, a far lower power consumption and long life expectancy.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al (US 2005/0194674) in view of Williams (US 4,910,643). Thomas discloses all claim limitations in claim 1 above but fails to disclose wherein the spacer is about 1 mm away from the third and fourth sides of the first die. Williams discloses the use of pads of various sizes (col. 4, lns. 50-60) that if incorporated with the disclosure of Thomas would achieve the distance claimed by the applicant. One would have been so motivated to modify Thomas with the pads of Williams to produce a much more economical circuit but also allow the spacer to cover all but 1 mm of the die.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al (US 2005/0194674) in view of Katagiri et al (2002/0185744) and in further view of He et al (US 2004/0039859). Thomas discloses an active circuitry on an upper surface (Fig. 1; 116), the semiconducting device further including a spacer (Fig. 1; 122) covering the active circuitry on the upper surface (Fig. 1; 116) and a die (Fig. 1; 112) that is stacked onto the spacer (Fig. 1; 122), the spacer extending from a first side of the die to an opposing second side of the die and extending near a third side of the die and an opposing fourth side of the die such that the active circuitry is exposed near the

third and fourth sides of the die (see Fig. 1). Thomas fails to disclose wherein the first die includes a flash memory array. Katagiri, however, does teach where the first die includes a flash memory (para. 0069). However, both Thomas and Katagiri fails to disclose an electronic system comprising a buss; a memory coupled to the buss and a semiconducting device that is electrically connected to the buss. He does disclose a buss (42); a memory (50) coupled to the buss (42) (para. 0023-0026) and a semiconducting device that is electrically connected to the buss (pg. 3, #15). One would have been so motivated to modify Thomas and Katagiri with the electronic system of He to incorporate all separate structures to produce a general-purpose electronic system.

Regarding claims 23-24, the prior art of Thomas, Katagiri and He teach all claim limitations as described above. Furthermore, Thomas and Katagiri disclose wherein the spacer includes at least one section that extends to the third side of the flash memory such that the active circuitry is only partially exposed near the third side of the flash memory (claim 23) and wherein the spacer includes at least one section that extends to the fourth side of the flash memory such that the active circuitry is only partially exposed near the fourth side of the flash memory (claim 24) (see Fig. 1-Thomas, para. 0069-Katagiri).

Regarding claim 26, the prior art of Thomas, Katagiri and He teach all claim limitations as described above. Furthermore, Thomas discloses wires (128) bonded to pads (129) that are part of the exposed active circuitry near the third and fourth sides of the flash memory, the wires being electrically coupled to the substrate (see Fig. 1).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al (US 2005/0194674) in view of Katagiri et al (2002/0185744), He et al (US 2004/0039859) and in further view of Li et al (US 6,493,861). The prior art of Thomas, Katagiri and He teach all claim limitations as described above but fails to disclose a voltage source electrically coupled to the semiconducting device. Li does disclose a voltage source electrically coupled to the semiconducting device (col. 13, lns 36-67). One would have been so motivated to modify Thomas, Katagiri and He with the voltage source of Li that results in less voltage drop and a much more efficient power delivery system.

Response to Arguments

Applicant's arguments with respect to claims 1-11 and 22-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deloris Bryant whose telephone number is (571) 272-8670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

dsb

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